ABSTRACT

A process for fabricating a novel random access memory (RAM) capacitor in a shallow trench isolation (STI). The method utilizes a novel node photoresist mask for plasma etching recesses in the STI that prevents plasma-etch-induced defects in the substrate. This novel photoresist mask is used to etch bottle-shaped recesses in the STI under a first hard mask. After forming bottom electrodes in the recesses and forming an interelectrode dielectric layer, a conducting layer is deposited sufficiently thick to fill the recesses and to form a planar surface, and a second hard mask is deposited. The conducting layer is patterned to form the capacitor top electrodes. This reduced topography results in reduced leakage currents when the gate electrodes are formed over the capacitor top electrodes.